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Description

METHOD AND APPARATUS FOR IMAGE FRAME SYNCHRONIZATION

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to video display devices, and more particularly, to converting from a first display resolution to a second display resolution using image frame synchronization.

[0003] 2. Description of the Prior Art

[0004] Graphics systems display images on display screens. For example, a computer system may display an image on a flat-panel monitor. Television systems and cameras are additional examples of such graphics systems. To achieve the display of an image, the image is generally represented by image data (e.g., RGB data), and display signals are generated from the image data. The standard VGA format is 640 pixels wide by 480 pixels high. The display

signals for a standard VGA monitor must redraw the entire screen at least 60 times a second to avoid causing a flicker that can be seen by the human eye and to allow smooth motion of the image. This period is called the refresh rate and the screen refresh process typically begins in the top left corner and displays 1 pixel at a time from left to right. When the current row is finished the next row is displayed in the same manner until all rows have been displayed and the refresh process begins again.

[0005] Fig.1 shows a timing diagram 10 of the typical display signals for a VGA system. The display signals including a vertical sync signal VS indicating the beginning of each screen, also called a frame; a horizontal sync signal HS indicating the beginning of each row, also called a horizontal line; and a data enable line indicating the pixel data in each scan line. As shown in Fig.1, a first frame starts at the first rising edge E1 of the vertical sync signal and a second frame starts at the second rising edge E2.

[0006] As graphics systems continue to have higher and higher display resolutions, a need emerges to convert image data from a first resolution to a second resolution. Graphics systems typically use special circuitry to convert image resolution. Examples of such circuitry include the well-

known graphics controller chips typically housed on a motherboard of a computer system and LCD control chip sets provided with LCD panels and video cameras. Frame rate conversion is a common technique well known in the art and involves outputting a destination display signal at a different frame rate than the incoming display signal. Because the incoming and outgoing frame rates are different, a large memory is needed to store incoming and outgoing pixel data, increasing the cost and complexity of the graphics system.

[0007] With the advance of graphics systems technology, a larger degree of tolerance for the outgoing frame rate is acceptable. For most new displays, it is sufficient to use the same frame rate for the source display signals and the destination display signals, simplifying the design and reducing the required memory. This technique is called frame synchronization and involves generating a destination frame for each source frame received and outputting the destination frames at the same rate as the source frames are received.

[0008] A significant timing problem is inherent in frame synchronization. The source signals contain both visible horizontal lines and non-visible horizontal lines. Resolution is

normally specified in terms of visible pixels only but, in reality, there are the additional non-visible horizontal lines and non-visible pixels at the ends of the visible horizontal lines. If a resolution is converted from x to y then the ratio of x:y must also hold for the non visible horizontal lines. An example of where difficulties are encountered is when converting frame signals for a typical VGA system. As previously mentioned, the typical VGA system is 640x480, or 480 horizontal lines; however, in reality there are approximately 504 horizontal sync signals sent for each vertical sync signal. The extra horizontal lines are not visible but are present to allow the display device time to return to the upper left corner before beginning the next refresh cycle. The ratio of visible source horizontal lines to visible destination horizontal lines must be equal to the ratio of total source horizontal lines to total destination horizontal lines. If a destination display device having a resolution of 1280x1024 is to be used, this equates to 1024/480*504 or a total of 1075.2 destination horizontal lines. The value of the destination horizontal lines must be an integer but if this value is rounded up, overflow occurs because the source frame rate will be higher than the destination frame rate. Conversely, if this value is

rounded down, underflow occurs because the source frame rate will be lower than the destination frame rate.

SUMMARY OF INVENTION

[0009] It is therefore a primary objective of the claimed invention to provide a method and apparatus for image frame synchronization, to solve the above-mentioned timing problem to prevent overflow and underflow.

[0010] According to the claimed invention, a method of frame synchronization for converting a source frame signal to a destination frame signal is disclosed. The source frame signal is received at a first frame rate and the destination frame signal is output at a second frame rate. The destination frame signal includes a plurality of horizontal lines and each of the horizontal lines includes a plurality of pixel data. The method comprises outputting the destination frame signal according to the source frame signal; and adjusting the number of the pixel data of at least one of the horizontal lines such that the first frame rate and the second frame rate are substantially the same.

[0011] According to the claimed invention, an apparatus for converting a source frame signal to a destination frame signal is disclosed. The source frame signal is received at a first frame rate and the destination frame signal is output at a

second frame rate. The destination frame signal includes a plurality of horizontal lines and each of the horizontal lines includes a plurality of pixel data. The apparatus comprises a buffer for storing at least a part of the pixel data and a converter for adjusting the number of the pixel data of at least one of the horizontal lines such that the first frame rate and the second frame rate are substantially the same.

[0012] It is an advantage of the claimed invention that by adjusting the number of pixel data in the last horizontal line, a last horizontal sync signal and a vertical sync signal can be made to be within in a predetermined time period.

[0013] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0014] Fig.1 is a timing diagram of typical video signals according to the prior art.

[0015] Fig.2 is an image frame according to the present invention.

[0016] Fig.3 is a timing diagram showing the timing constraint of

the horizontal sync signal to the vertical sync signal.

[0017] Fig.4 is a frame synchronization apparatus according to the present invention.

[0018] Fig.5 is a flowchart showing the method of image frame synchronization according to the present invention.

DETAILED DESCRIPTION

[0019] Fig.2 shows a destination frame 20 according to the present invention. The destination frame 20 includes a first horizontal line 24, a first visible horizontal line 26, a last visible horizontal line 28, and a last horizontal line 30. The horizontal lines contain pixel data comprising both non-visible porch signals and visible pixel signals. For this reason, Fig.2 also includes a visible region 22 indicating the pixel signals that are visible and displayed on the display device. The visible region 22 encloses the pixel signals and all pixel data outside the visible region are the non-visible porch signals. As an example, the visible region 22 can be thought of as the video screen of a computer monitor or an LCD panel. Throughout the remainder of the disclosure, the term pixel data refers to the both the non-visible porch signals and the visible pixel signals.

[0020] By adjusting the number of non-visible porch signals for

the image frame20, the underflow and overflow problems of the prior art are solved. When an underflow condition exists, the source frame rate is slightly lower than the destination frame rate. Additional non-visible porch signals are added to the horizontal line of the destination image frame to increase the total number of the pixel data of the destination image frame and slow down the destination frame rate. The number of additional porch signals added ensures that the source frame rate is the same as the destination frame rate. The additional porch signals are distributed among the horizontal lines of the image frame. In Fig.2, extra porch signals have been added to horizontal lines 32, 34, and 36. Similarly, to correct an overflow condition, some non-visible porch signals could be removed from some of the horizontal lines in the destination image frame, thereby decreasing the total number of the pixel data of the destination image frame and increasing the destination frame rate.

[0021] Because extra porch signals are added (or removed) at the end of the horizontal line in the non-visible section, by the time the display device reaches the end of the horizontal line, it has already drawn the horizontal line and automatically accounts for a slight delay (advance) in re-

ceiving the next horizontal sync signal. The need for the non-visible porch signals originally came from CRT display devices needing time to move to the starting position of the next horizontal line. For many digital display devices the porch signals are not a critical element of the display and the number can be slightly adjusted on a horizontal line by horizontal line basis. However, due to the internal design of some display devices, for example some LCD panels, there may be a constraint that the number of pixel data in each horizontal line needs to be an even number. This is due to the way the clocking system works in the LCD panel as some panels use a divide by two clock and work with pixels in groups of two. There also exist a number of panels that use a divide by four clock and for these particular panels the number of pixel data in each horizontal line needs to be divisible by four.

[0022] Fig.3 shows a timing diagram 39 of the relationship between the vertical sync signal VS and the horizontal sync signal HS. For some destination display devices, particularly some LCD panels, there is an additional hardware restriction limiting the maximum time T_{LIMIT} between the last horizontal sync signal and the vertical sync signal. The start of the last horizontal sync signal HS, represented

by a third rising edge E3, must be within a time T_{LIMIT} of the start of the vertical sync signal VS, represented by a fourth rising edge E4. For some display devices, the video signals need to comply with this restriction or the display device will not function properly.

[0023] To satisfy this timing requirement, the number of porch signals in the last horizontal line of the destination frame is reduced and in order to maintain the destination frame rate, at least one of the other horizontal lines in the destination frame has its number of porch signals increased. When correcting the timing between the horizontal sync signal and the vertical sync signal, the total number of pixel data in the destination frame remains constant so as to not affect the destination frame rate.

[0024] Fig.4 shows a frame synchronization apparatus 40 according to the present invention. The frame synchronization apparatus 40 includes a converter 42 and a First-In-First-Out (FIFO) buffer 44. Source video signals at a first display resolution are received at a first frame rate and stored in the FIFO 44. The FIFO 44 stores the incoming pixel data until it is read out of the FIFO 44 by the converter 42, of which the structure and the operation are well-known by people skilled in the art, to convert from

the first resolution to the second resolution. For each image frame in the source video signals, the converter 42 generates a destination frame in the destination video signals at a second frame rate. It should also be noted that although the FIFO 44 is used as a buffer, this is for example only and any buffer implementation can be used.

[0025] If the first frame rate is higher than the second frame rate, pixel data will overflow the FIFO 44. To increase the second frame rate, the converter 42 decreases the number of non-visible porch signals in at least one of the horizontal lines of the destination frame such that the FIFO 44 is no longer in the overflow condition. When some porch signals are removed from the destination frame, the frame takes less time to transmit and the second frame rate is increased. If the first frame rate is lower than the second frame rate, pixel data will be read out of the FIFO 44 too quickly and the FIFO 44 will underflow. To decrease the second frame rate, the converter 42 increases the number of porch signals in at least one of the horizontal lines in the destination frame such that the FIFO 44 is no longer in the underflow condition. The converter 42 adjusts the number of non-visible porch signals in the destination frame such that the pixel data in the FIFO 44 remains

above a minimum level and below a maximum level. In this stable condition, the first frame rate and the second frame rate are substantially the same.

[0026] To ensure compatibility with some destination display devices, the converter 42 may be required to make the number of pixel data in each horizontal line divisible by two or four depending on if the destination display device uses a divide by two or a divide by four clock respectively. Additionally, the number of porch signals in the last horizontal line of the destination frame may need to be reduced to allow the time between the last horizontal sync signal and the vertical sync signal to be within a maximum allowable time limit. These adjustments are dependent on the particular destination display and, regardless of whether required or not, the converter 42 ensures that the FIFO 44 is not in an overflow or underflow condition.

[0027] Fig.5 shows a flowchart 50 illustrating the method of frame synchronization according to the present invention. The flowchart 50 comprises the following steps:

[0028] Step 52:Determine if the first frame rate is equal to the second frame rate. A simple method for determining whether the first frame rate is equal to the second frame rate is checking whether incoming pixel data in a buffer or

memory remains above a minimum level and below a maximum level. In this stable condition, the first frame rate and the second frame rate are substantially the same so proceed to step 60, otherwise proceed to step 54.

[0029] Step 54:Check for an overflow condition. If an overflow condition exists then proceed to step 58, if not (underflow) then proceed to step 56.

[0030] Step 56:Increasing the number of porch signals increases the size of the destination frame and lowers the second frame rate. For some destination displays, it may also be necessary to ensure that the number of pixel data in each horizontal line is a multiple of two or a multiple of four. Proceed to step 52.

[0031] Step 58:Decreasing the number of porch signals decreases the size of the destination frame and increases the second frame rate. For some destination displays it may also be necessary to ensure that the number of pixel data in each horizontal line is a multiple of two or a multiple of four. Proceed to step 52.

[0032] Step 60:Determine if the timing requirements for the horizontal sync signal and the vertical sync signal of the destination display are satisfied. If satisfied then end, if timing adjustment is needed then proceed to step 62.

[0033] Step 62:Decrease the number of porch signals in the last horizontal line. Because the second frame rate must remain constant, the total number of porch signals that are added to other horizontal lines must be equal to the number of porch signals removed from the last horizontal line. Proceed to step 60.

[0034] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended claims.